

FIG. 1

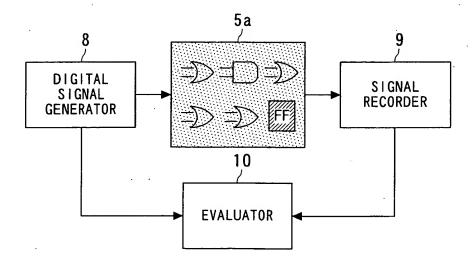


FIG. 2

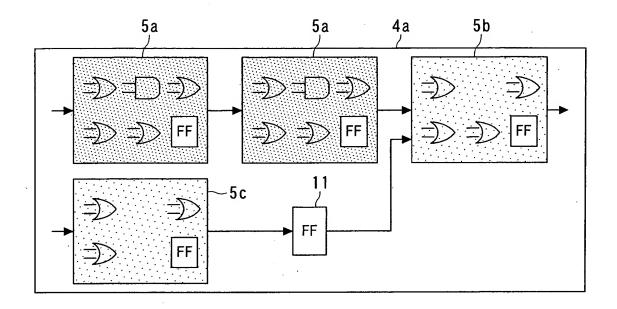


FIG. 3

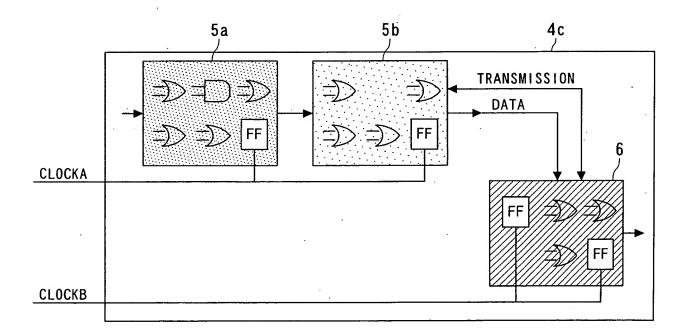


FIG. 4

VHDL STATEMENT

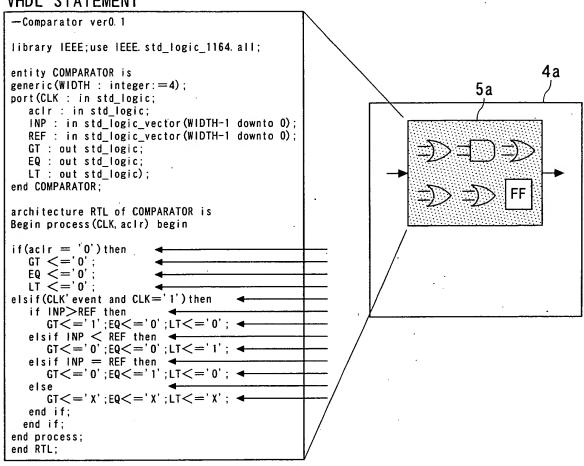
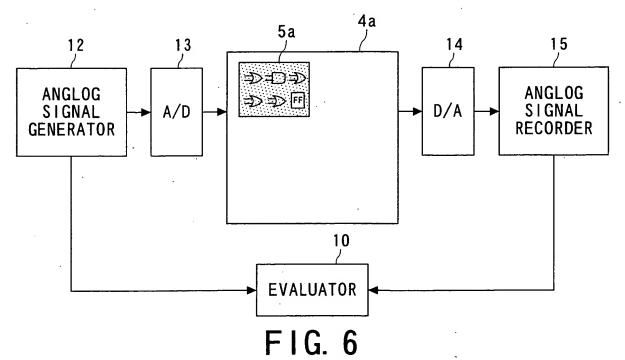


FIG. 5



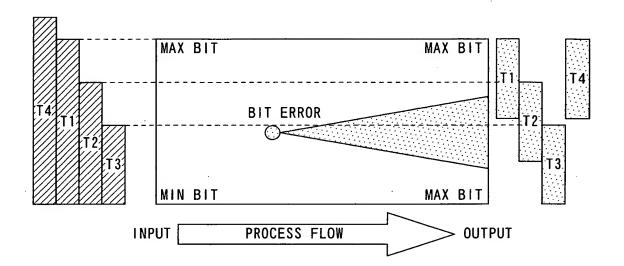


FIG. 7

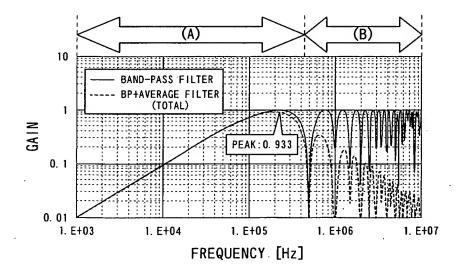


FIG. 8

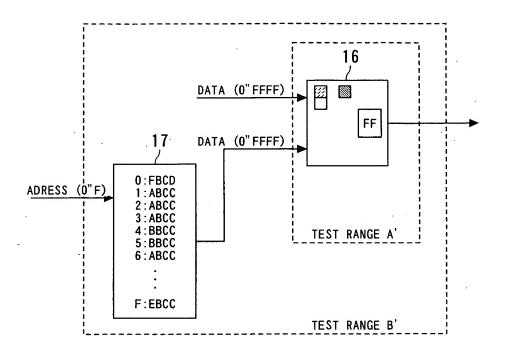


FIG. 9

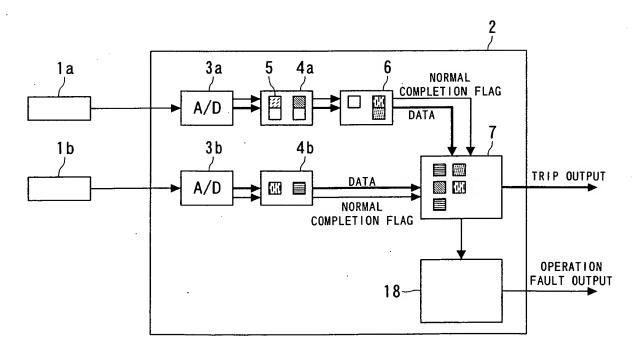


FIG. 10

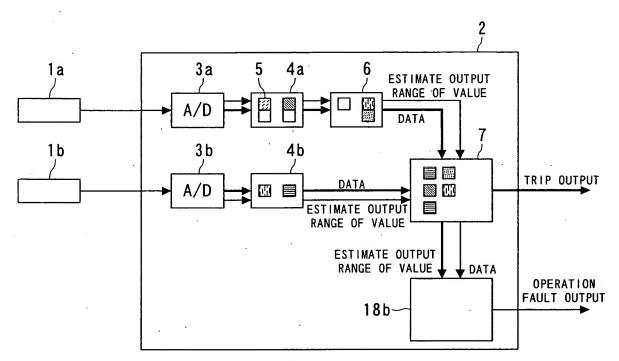
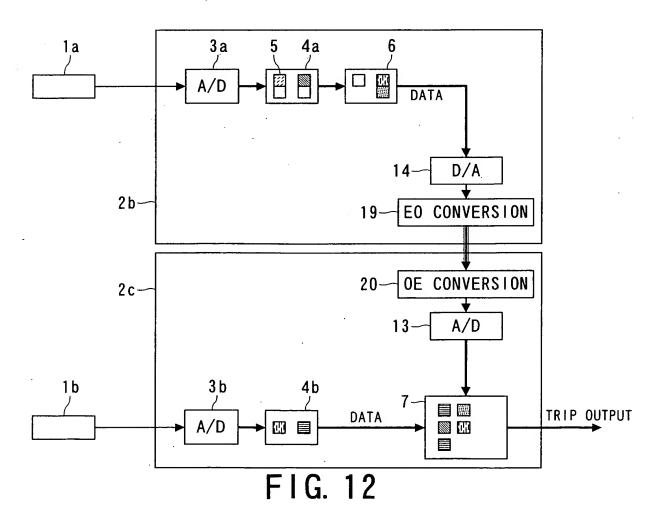


FIG. 11



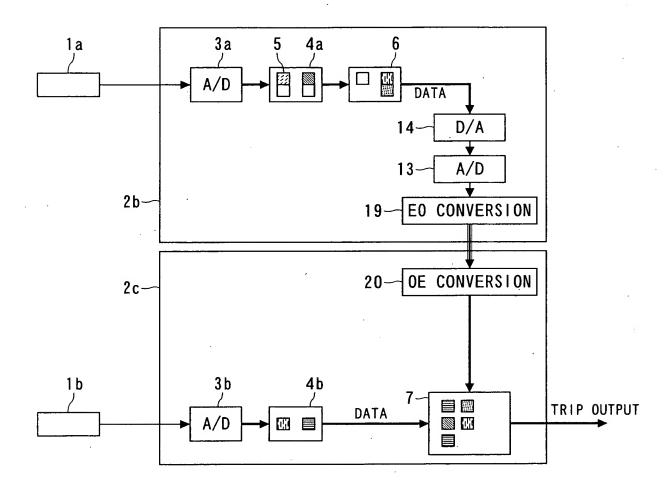


FIG. 13

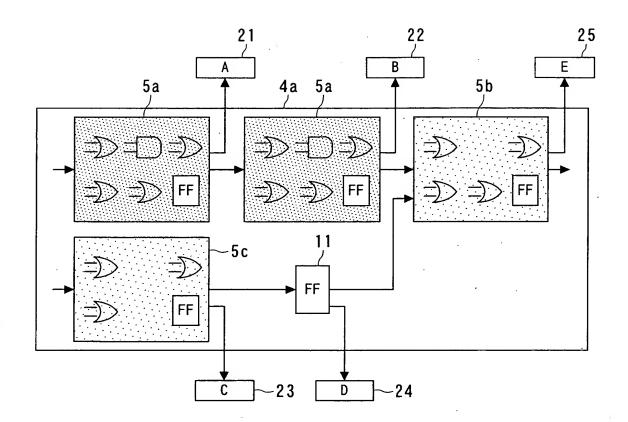


FIG. 14

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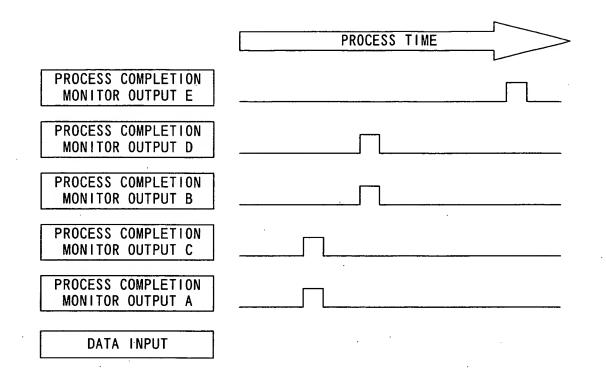


FIG. 15

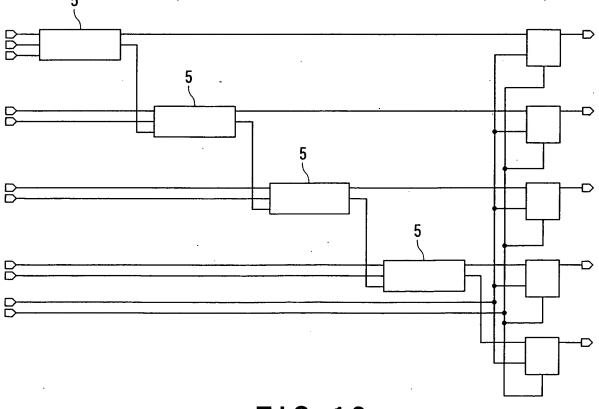


FIG. 16